

<b>TITLE</b> <b>QSFP28 100G to 4x25G AOC</b> <b>(Active Optical cable)</b>	<b>DOC No.</b>	<b>DTRX-200725</b>
	<b>REVISION :</b> <b>01</b>	<b>AUTHORIZED BY :</b> <b>Albert Lin</b>
	<b>DATE :</b> <b>2020.07.24</b>	<b>CLASSIFICATION :</b> <b>Active Optical Cable</b>

### 1. Purpose

This document validates solely for the product of Jess Link, QSFP28 100Gbps Active Optical Cable (AOC), with its basic information and electronic characteristics. With continuous performance improvement purpose, the document might subject to change without notice.

### 2. Feature

- Support 4x25GBASE-SR Application
- Compliant to QSFP28 MSA SFF-8636 and SFP28 MSA SFF-8431 and SF-8472
- Multi rate of up to 25.78125Gbps per lane
- +3.3V single power supply
- Low power consumption
- UL certification cables (optional)
- Operating case temp Commercial: 0°C to +70 °C
- RoHS 6/6 compliant

### 3. Applications

- 4x25GbE-SR
- Other Optical Links

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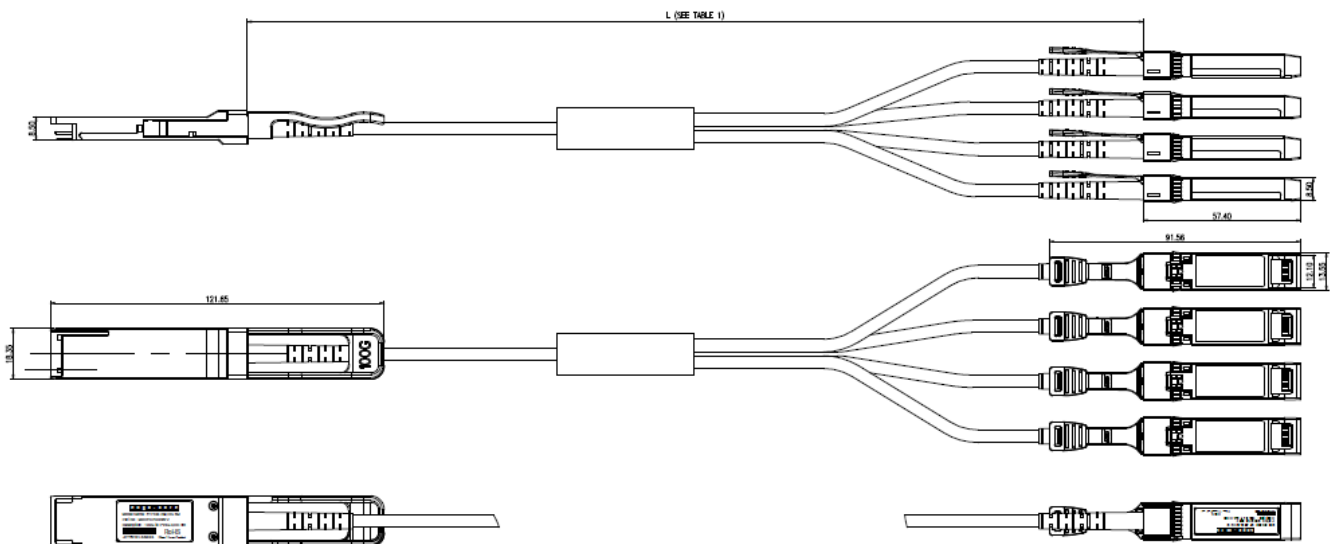
#### 4. Product Description

##### 4.1 Product Name And Series Number(s)

##### 100G QSFP28 to 4xSFP28 AOC

Category	Bit Rate	Laser(nm)	Distance	Fiber Type	DDMI	Connector	Temp
QSFP28	103.125	850	1~50m	MMF	YES	N/A	C

##### 4.2 Dimensions, Materials, Platings and Marking



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## 5. Absolute Maximum Rating

Parameter	Symbol	Min	Typical	Max	Unit	Note
Supply Voltage	V <sub>CC3</sub>	-0.5	-	+3.6	V	
Storage Temperature	T <sub>s</sub>	-10	-	+70	°C	
Operating Humidity	RH	+5	-	+85	%	1

Note 1:Case Temperature

## 6. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Case Operating Temperature	T <sub>c</sub>	0	-	+70	°C	
Power Supply Voltage	V <sub>CC</sub>	3.14	3.3	3.47	V	
Power Dissipation per QSFP28	P <sub>d</sub>	-	-	2.5	W	
Power Dissipation per SFP28	P <sub>d</sub>	-	-	1.0	W	1
Bit Rate per Lane	BR	10.3125	25.78125	-	Gbps	

Note 1:per Terminal

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## 7. Optical and Electrical Characteristics

### QSFP28

Parameter		Symbol	Min	Typ	Max	Unit
<b>Electrical Characteristics</b>						
ModSelL	Module Select	VOL	0	-	0.8	V
	Module Unselect	VOH	2.5	-	VCC	V
LPMMode	LowPower Mode	VIL	0	-	0.8	V
	Normal Operation	VIH	2.5	-	V <sub>CC</sub> +0.3	V
ResetL	Reset	VIL	0	-	0.8	V
	Normal Operation	VIH	2.5	-	V <sub>CC</sub> +0.3	V
ModPrsL	Normal Operation	VOL	0	-	0.4	V
IntL	Interrupt	VOL	0	-	0.4	V
	Normal Operation	VoH	2.4	-	VCC	V
<b>Electrical Transmitter Characteristics</b>						
Differential Date Input Swing		V <sub>out</sub>	200	-	1600	mV
Output Differential Impedance		Z <sub>D</sub>	90	100	110	Ω
<b>Electrical Receiver Characteristics</b>						
Differential Data Output Swing		V <sub>in,P-P</sub>	200	-	800	mV <sub>PP</sub>
Bit Error Rate		BER			E-12	
Input Differential Impedance		Z <sub>IN</sub>	90	100	110	Ω

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**SFP28**

Parameter		Symbol	Min	Typ	Max	Unit
<b>Electrical Transmitter Characteristics</b>						
Differential Data Input Swing		$V_{in,P-P}$	200	-	1600	mV <sub>PP</sub>
Input Differential Impedance		$Z_{IN}$	90	100	110	$\Omega$
Tx_Fault	Normal Operation	$V_{OL}$	0	-	0.8	V
	Transmitter Fault	$V_{OH}$	2.0	-	$V_{CC}$	V
Tx_Disable	Normal Operation	$V_{IL}$	0	-	0.8	V
	Laser Disable	$V_{IH}$	2.0	-	$V_{CC}+0.3$	V
<b>Electrical Receiver Characteristics</b>						
Differential Date Output		$V_{out}$	400	-	800	mV
Bit Error Rate		BER	-	-	E-12	-
Output Differential Impedance		$Z_D$	90	100	110	$\Omega$
Rx_LOS	Normal Operation	$V_{OL}$	0	-	0.8	V
	Lose Signal	$V_{oH}$	2.0	-	$V_{CC}$	V

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**8. QSFP+ Module Pad Assignments and Descriptions**

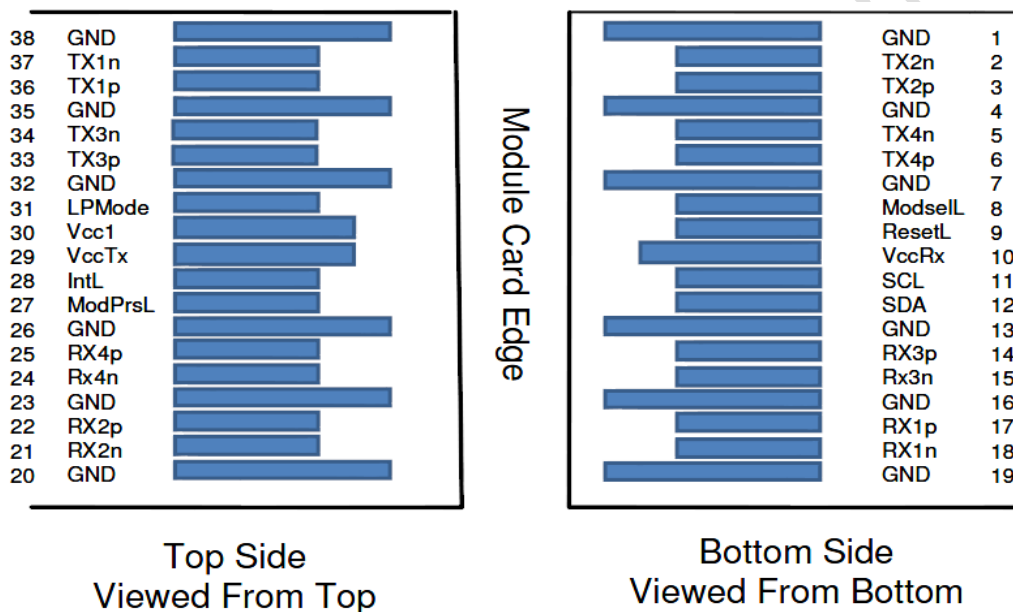


Figure 1, Pin View for QSFP28

**Pin Function Definitions for QSFP28**

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	

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12	SDA	2-wire serial interface data	
13	GND	Ground	2
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Note 1: Circuit ground is internally isolated from chassis ground.

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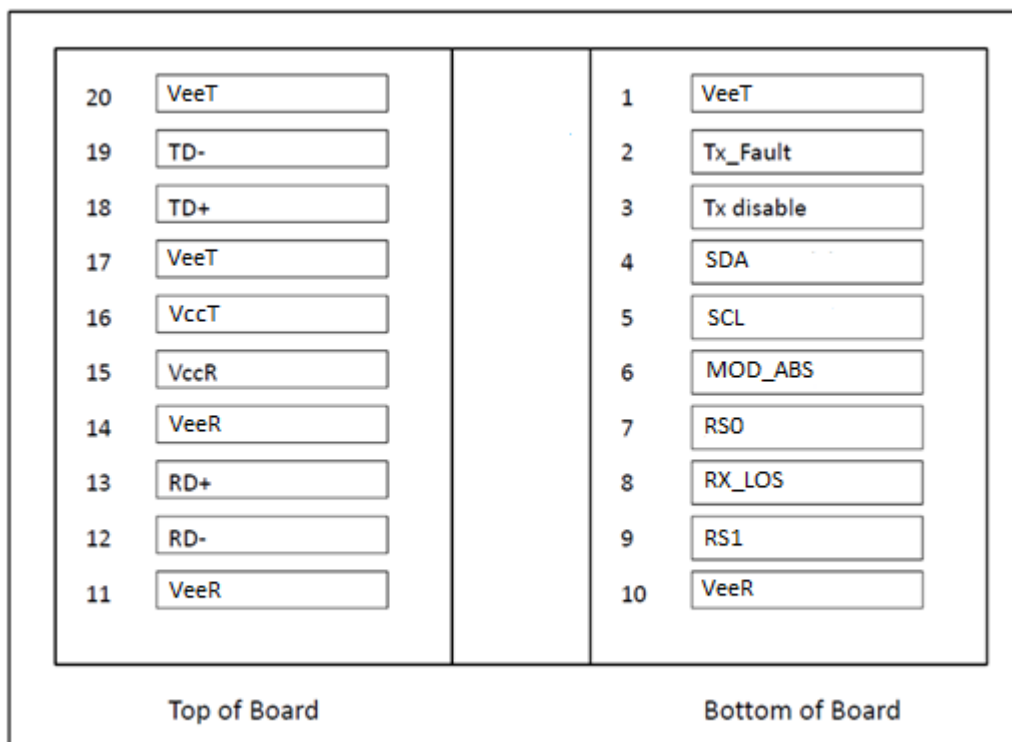


Figure 2, Pin View for SFP28

**Pin Function Definitions**

Pin	Symbol	Description	Notes
1	VeeT	Module Transmitter Ground	Note1
2	TX_Fault	Module Transmitter Fault	Note2
3	TX_Disable	Transmitter Disable; Turns off transmitter laser output	Note3
4	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 as defined in the INF-8074i)	Note4
5	SCL	2-wire Serial Interface Clock (Same as MOD-DEF1 as defined in the INF-8074i)	Note4
6	MOD_ABS	Module Absent, connected to VeeT or VeeR in the module	Note5
7	RS0	Rate Select 0, optionally controls SFP+ module receiver. When High input data rate 10.3GBd and when LOW input	



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		data rate 1.25 GBd.	
8	RX_LOS	Receiver Loss of Signal Indication (In FC designated as RX_LOS, in SONET designated as LOS, and in Ethernet designated as Signal Detect)	Note2
9	RS1	Rate Select 1, optionally controls SFP+ transmitter. When High input data rate 10.3GBd and when LOW input data rate 1.25 GBd.	
10	VeeR	Module Receiver Ground	Note1
11	VeeR	Module Receiver Ground	Note1
12	RD-	Receiver Inverted Data Output	
13	RD+	Receiver Non-Inverted Data Output	
14	VeeR	Module Receiver Ground	Note1
15	VccR	Module Receiver 3.3 V Supply	
16	VccT	Module Transmitter 3.3 V Supply	
17	VeeT	Module Transmitter Ground	Note1
18	TD+	Transmitter Non-Inverted Data Input	
19	TD-	Transmitter Inverted Data Input	
20	VeeT	Module Transmitter Ground	Note1

**Notes:**

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10kohms to Host\_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10kohms to VccT in the module.
4. See sff-8431 4.2 2-wire Electrical Specifications .
5. This pin shall be pulled up with 4.7k-10kohms to Host\_Vcc on the host board.

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9. Recommended Circuit

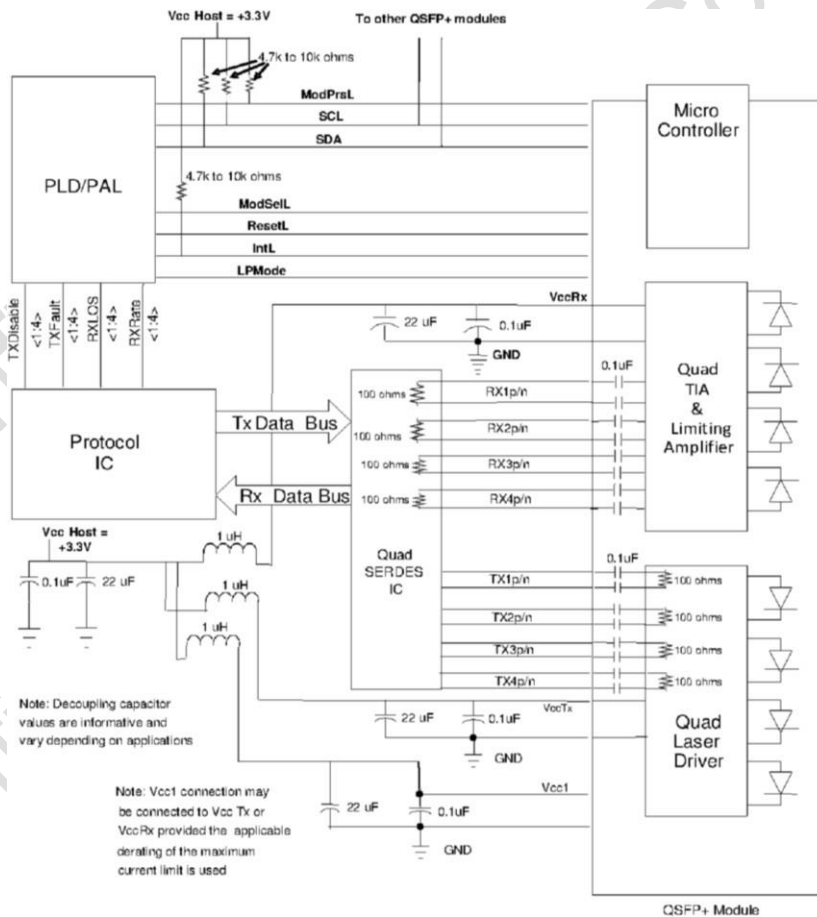


Figure 3, Recommended Interface Circuit for QSFP28

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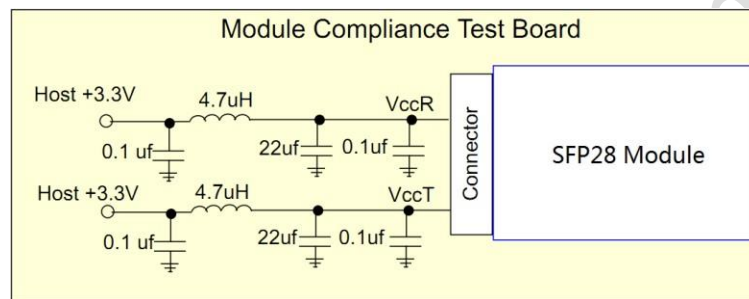


Figure 4, Recommended Host Board Power Supply Circuit for SFP28

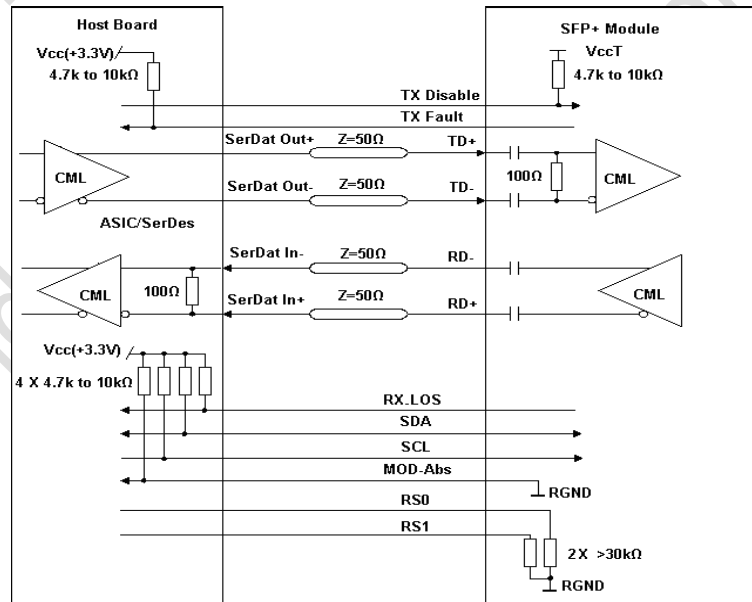


Figure 5, Recommended Interface Circuit for SFP28

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**10. Monitoring Specification**

<b>2-Wire Serial Address 1010000x</b> <b>Lower Page 00h</b>	
0	Identifier
1- 2	Status
3- 21	Interrupt Flags
22- 33	Free Side Device Monitors
34- 81	Channel Monitors
82- 85	Reserved
86- 98	Control
99	Reserved
100-104	Hardware Interrupt Pin Masks
105-106	Vendor Specific
107	Reserved
108-110	Free Side Device Properties
111-112	Assigned for use by PCI Express
113	Free Side Device Properties
114-118	Reserved
119-122	Password Change Entry Area (Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte

Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h	
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds	
129-191 Base ID Fields	129 AST Table Length (TL)		176-223 Channel Thresholds	
192-223 Extended ID	130-131 Application Code Entry 0			224 Tx EQ & Rx Emphasis Magnitude ID
	132-133 Application Code Entry 1			
	134-253 other entries			
224-255 Vendor Specific ID	254-255 Application Code Entry TL	225 RX output amplitude indicators	226-241 Channel Controls	
			242-251 Channel Monitor Masks	
			252-255 Reserved	

**Figure 6, Memory Map for QSFP28**

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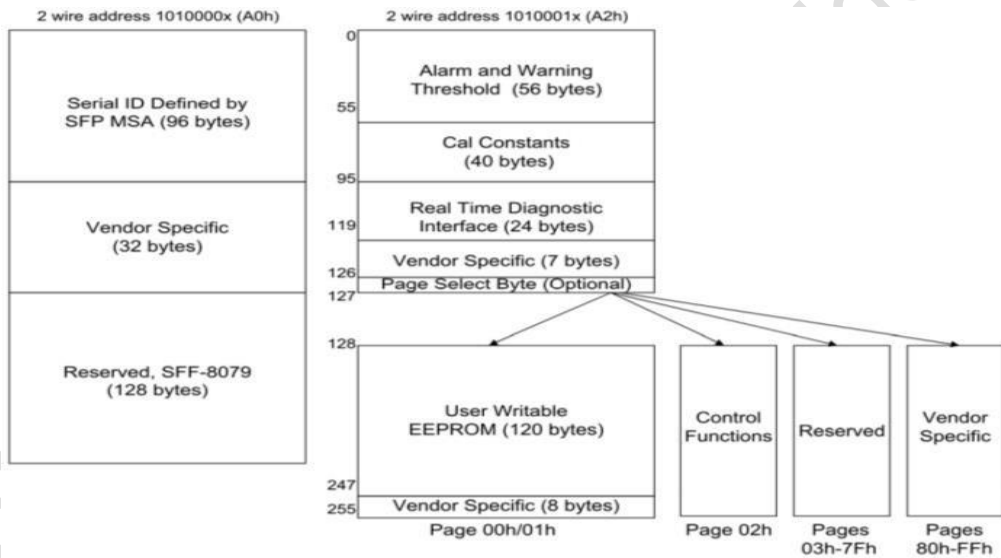


Figure 7, Memory Map for SFP28

**11. Modification History**

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2020.07.24	Albert Lin	Mike Sun